WHAT IS CLAIMED IS:

1. A semiconductor wafer having an active surface, comprising:

a plurality of dice, each die having a plurality of contact pads formed on the active surface of the wafer;

a resilient layer disposed on the active surface of said wafer, said resilient layer having a plurality of vias formed therethrough, wherein sidewalls of at least some of said plurality of vias are tapered at an angle relative to the active surface of said wafer;

a plurality of under bump metallization stacks, each under bump metallization stack including a nickel-vanadium layer and a copper layer, wherein the nickel-vanadium layer is directly atop and in substantial contact with an associated contact pad and the copper layer is directly atop and in substantial contact with the nickel-vanadium layer, said under bump metallization stack being arranged such that at least some portion of the under bump metallization stack overlies a portion of said resilient layer; and

a plurality of solder bumps, each solder bump being formed on an associated under bump metallization stack.

2. The semiconductor wafer of claim 1, wherein said at least one resilient layer comprises benzocyclobutene or a polyimide.

3. The semiconductor wafer of claim 1, wherein one or more of said plurality of under bump metallization stacks has a total thickness of less than about 15 kilo-angstroms.

4. The semiconductor wafer of claim 3, wherein one or more of said plurality of under bump metallization stacks has a total thickness of less than about 12 kilo-angstroms.

5. The semiconductor wafer of claim 1, further comprising:

a passivation layer disposed on the active surface of said wafer, wherein at least a portion of said passivation layer is located between the active surface of said wafer and said resilient layer.

6. The semiconductor wafer of claim 5, wherein said passivation layer comprises a compound selected from the group consisting of silicon dioxide and silicon nitride.

7. The semiconductor wafer of claim 5, wherein said passivation layer comprises a plurality of passivation layer vias formed therethrough, wherein each of said plurality of passivation layer vias define a perimeter that completely encloses the perimeter of a corresponding resilient layer via.

8. An integrated circuit device, comprising:

a plurality of contact pads formed on a first surface of said device;

a plurality of under bump metallization stacks, wherein one or more of said plurality of under bump metallization stacks each couple with an associated contact pad, and wherein each such under bump metallization stack comprises a plurality of metal or alloy layers, none of which are an aluminum layer, a titanium layer or a chromium layer.

9. The integrated circuit device of claim 8, further comprising:

a resilient layer disposed on said first surface, said resilient layer having a plurality of vias formed therethrough, wherein one or more of said plurality of vias defines a primary axis extending therethrough and one or more sidewalls that are not substantially parallel to said primary axis.

10. The integrated circuit device of claim 8, wherein at least a portion of said plurality of under bump metallization stacks each comprise at least one layer selected from the group consisting of copper and nickel-vanadium.

11. The integrated circuit device of claim 10, wherein at least a portion of said plurality of under bump metallization stacks each comprise a copper layer directly atop and in substantial contact with a nickel-vanadium layer, which is in turn directly atop and in substantial contact with an associated contact pad.

12. The integrated circuit device of claim 8, wherein one or more of said plurality of under bump metallization stacks has a total thickness of less than about 15 kilo-angstroms.

13. The integrated circuit device of claim 8, further comprising:

a passivation layer disposed on said first surface, wherein at least a portion of said at least one passivation layer is located between said first surface and said resilient layer.

14. The integrated circuit device of claim 13, wherein said passivation layer comprises a plurality of passivation layer vias formed therethrough, wherein one or more of said plurality of passivation layer vias each define a perimeter that completely encloses the perimeter of a corresponding resilient layer via.

15. The integrated circuit device of claim 8, further comprising:

a plurality of solder bumps, wherein one or more of said plurality of solder bumps are each coupled with an associated under bump metallization stack and an associated contact pad.

16. A method of manufacturing an integrated circuit device, the method comprising:

providing a semiconductor wafer having an active surface thereupon;

forming a plurality of contact pads on said active surface;

forming a resilient layer on said active surface;

forming a plurality of vias through said resilient layer, wherein at least a portion of said plurality of vias are each coupled with an associated contact pad;

forming a plurality of under bump metallization stacks, wherein at least a portion of said plurality of under bump metallization stacks are each coupled with an associated contact pad, and wherein at least a portion of said plurality of under bump metallization stacks each have a plurality of layers, none of which are an aluminum layer, a titanium layer or a chromium layer; and

forming a plurality of solder bumps, wherein at least a portion of said plurality of said solder bumps are each coupled with an associated under bump metallization stack and an associated contact pad.

17. The method of claim 16, wherein at least a portion of said plurality of resilient layer vias each defines a primary axis extending therethrough and one or more sidewalls that are not substantially parallel to said primary axis.

18. The method of claim 16, wherein at least a portion of said plurality of under bump metallization stacks each comprise a copper layer directly atop and in substantial contact with a nickel-vanadium layer, which is in turn directly atop and in substantial contact with an associated contact pad.

19. The method of claim 16, wherein one or more of said plurality of under bump metallization stacks have a total thickness of less than about 15 kilo-angstroms.

20. The method of claim 16, further comprising the step of:

forming at least one passivation layer on said active surface, wherein at least a portion of said at least one passivation layer is located between said active surface and said resilient layer.